

TN28HPCPlus on EDA Cloud 2.0 (1/4)

■ How to access TN28HPCPlus design collaterals?

- All TN28HPCPlus design collaterals are in the path:

- `/process/TN28HPCplus/IP` # for Cell-Based Design Kits
- `/process/TN28HPCplus/TECH` # for Full-Custom Design Flow

- TSRI provides both cadence, and synopsys platforms of TN28HPCPlus iPDK. iPDK path:

- `/process/TN28HPCplus/TECH/PDK/iPDK_CDNS` # for cadence-virtuoso platform
- `/process/TN28HPCplus/TECH/PDK/iPDK_SNPS` # for synopsys-customcompiler/Laker platform

TN28HPCPlus on EDA Cloud 2.0 (2/4)

■ How to invoke EDA tool, for example HSPICE?

- You must first “source” the cshell file (*.csh) of the eda tool you want to use.

- For example, if you want to use HSPICE, you must first to source “hspice.csh”.
 - Step1. open a terminal
 - Step2. type source /cad/synopsys/CIC/hspice.csh

- You can find all EDA Tool cshell files in the path:

`/cad/<vendor>/CIC/<toolname>.csh`

- For example:
 - source /cad/synopsys/CIC/hspice.csh # for using HSPICE
 - source /cad/cadence/CIC/IC6.csh # for using IC6.1

- Here is also an example cshell for your reference:

- source /process/TN28HPCPlus/TECH/1_TSRI/PDK/tn28hpcplus.cshrc

TN28HPCPlus on EDA Cloud 2.0 (3/4)

■ How many EDA tools on EDA Cloud 2.0?

- You can find all EDA Tools in following path:

`/cad/<vendor>/<tool>/cur` # link to default version

➤ For example:

➤ `/cad/cadence/IC/cur` -> IC_23.10.030

➤ `/cad/synopsys/hspice/cur` -> v2023.03

- If you can't find the EDA tool/version you need, please make a request via [TSRI Custom Consulting System](#).

TN28HPCPlus on EDA Cloud 2.0 (4/4)

How to access TN28HPCPlus document(PDF)?

- All documents(PDF) are stamped with watermark, and only read via browser(firefox).

<http://140.126.24.97/ecbs/edaCloud/init.action>

製程編號	位置	文件名稱	瀏覽
TN28HPCplu			
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_LO	TN28CLSP079_1_0_2P8	瀏覽
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_LO	cln28hpcp_1d8_elk_v1d0_2p8_corner_release_note	瀏覽
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_LO	cln28hpcp_1d8_elk_v1d0_2p8_statistical_release_note	瀏覽
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_LO	cln28hpcp_v1d0_usage_guide	瀏覽
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_RF	TN28CRSP025_1_0_2P2	瀏覽
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_RF	cln28hpcp_1d8_elk_v1d0_2p8_corner_release_note	瀏覽
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_RF	cln28hpcp_1d8_elk_v1d0_2p8_statistical_release_note	瀏覽
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_RF	cln28hpcp_v1d0_usage_guide	瀏覽
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_RF	crn28hpcp_1d8_elk_v1d0_2p2_release_note	瀏覽
TN28HPCplu	/TN28HPCplus/SPICE_MODE/SPICE_RF	crn28hpcp_1d8_elk_v1d0_2p2_usage_guide	瀏覽
TN28HPCplu	/TN28HPCplus/TechFile	N28_stdVia_Spec.19a	瀏覽
TN28HPCplu	/TN28HPCplus/TechFile	TN28CLLE002_1_9A	瀏覽

Apply Chip Implementation Service

- How to submit your GDS via TSRI “Tape-out Application”
 - You can upload your gds file via browser(firefox) on EDA Cloud 2.0

[http:// ecbs.tsri.org.tw/ecbs](http://ecbs.tsri.org.tw/ecbs)



Submit GDS on EDA Cloud 2.0

- How to submit your GDS via TSRI “Tape-out Application”
 - Following instruction, upload GDS, DRC result, and LVS result.
 - Both design-content, and TRF can be upload from your school/lab.

Step 4-1: 點選上傳檔案，開啟上傳檔案視窗，上傳設計資料等所需檔案。

上傳檔案列表：

檔案類型	格式說明	檔案名稱	上傳時間	檔案大小(kb)	檔案是否已上傳	上傳檔案
佈局圖檔	佈局圖檔(*.gds 或*.db)	test1.gds	2024/01/22 10:51:36	1503.232	已上傳檔案	<input type="button" value="上傳檔案"/>
設計內容	設定內容格式 (*.doc、*.docx 或*.docm)	NONE	NONE	NONE	尚未上傳檔案	<input type="button" value="上傳檔案"/>
DRC結果	DRC結果檔格式 (*.drc.summary 或*.rep)	NONE	NONE	NONE	尚未上傳檔案	<input type="button" value="上傳檔案"/>
LVS結果	LVS結果檔格式 (*.lvs.report 或*.rep)	NONE	NONE	NONE	尚未上傳檔案	<input type="button" value="上傳檔案"/>
TRF文件	上傳TRF文件檔 (TRF.doc、 TRF.docx、 TRF.docm、 trf.doc、trf.docx 或trf.docm)	NONE	NONE	NONE	尚未上傳檔案	<input type="button" value="上傳檔案"/>

TN28HPCplus DRC “HARD RULE”

- Your Layout(GDS) must be DRC CLEAN before tape-out.
 - These following are “HARD RULE”, and can’t be waived for any purpose.
 - TSMC has authority to reject any un-clarified DRC fail devices on tape-in date to guard the quality.

PO.W.2; OD.DN.3;
PO.S.45; OD.DN.3.1;
PO.S.12; AP.W.5;
PO.DN.2; AP.S.1;
PO.DN.3;
PO.DN.3.1;
PO.DN.4