NARLabs
國家實驗研究院

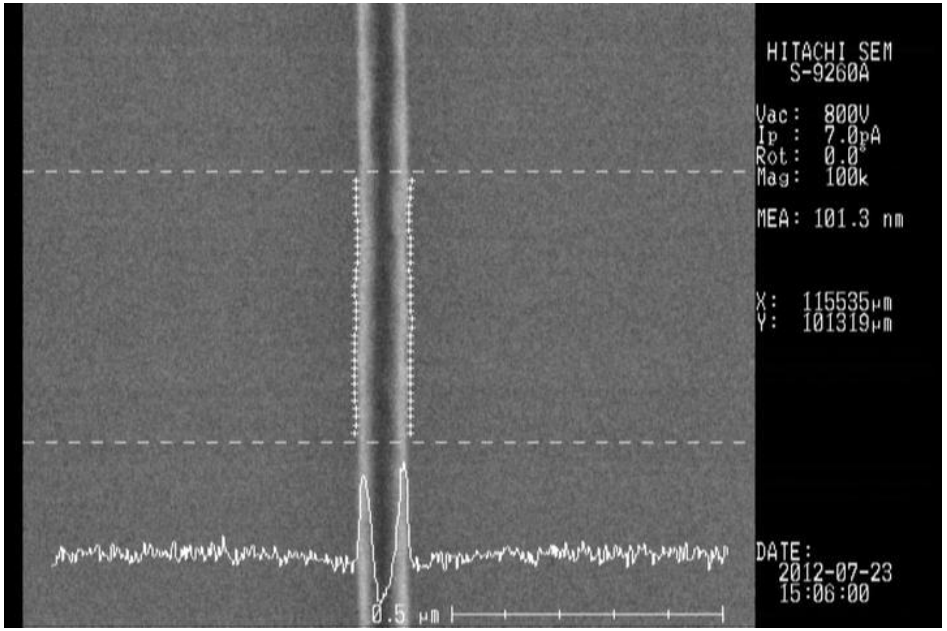
可變形束電子束曝光機
標準製程

NEB resist process sequence aim: ~380nm resist thickness

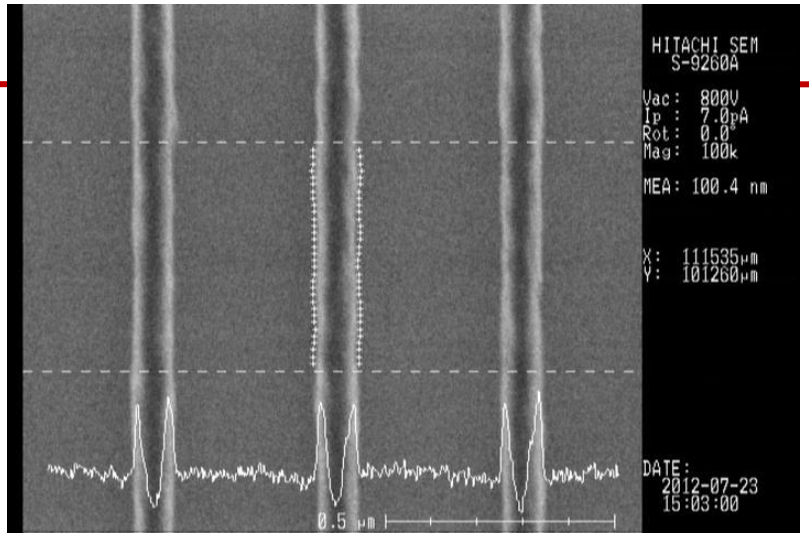
NARLabs

- Prime — HMDS 90°C
- Coating — 4400 rpm 30“
- Softbake — 110°C 120“
- Exposure — Base Dose 16µC/cm²
- Post Exposure Bake — 105°C 120“
- Development — AD-10 2.38% TMAH 60“ puddle
- Rinse — Di-Water
- Hardbake — 110°C 120“
  - Track ACT8 recipe
    - COT-NEB
    - DEV-NEB

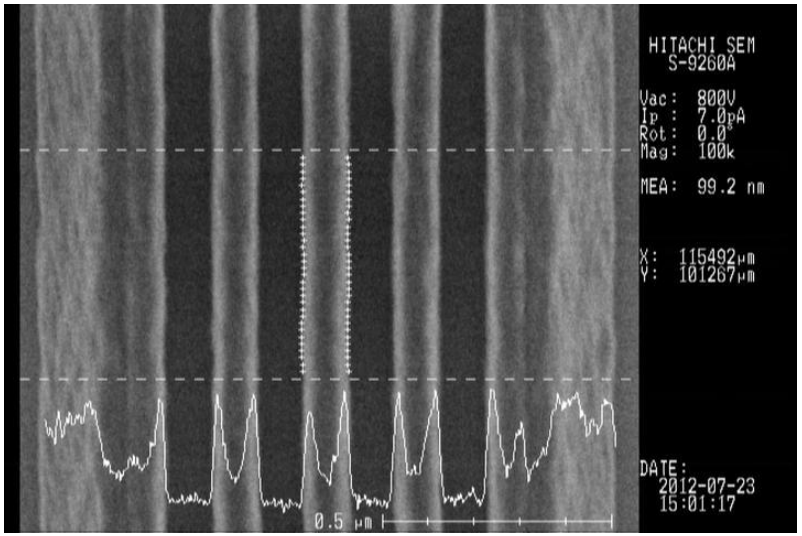
100 nm line



101.3 nm iso @12µC/cm²



101.7 nm L/S=1:3 @11.2µC/cm²



Collapse L/S=1:1 @12µC/cm²

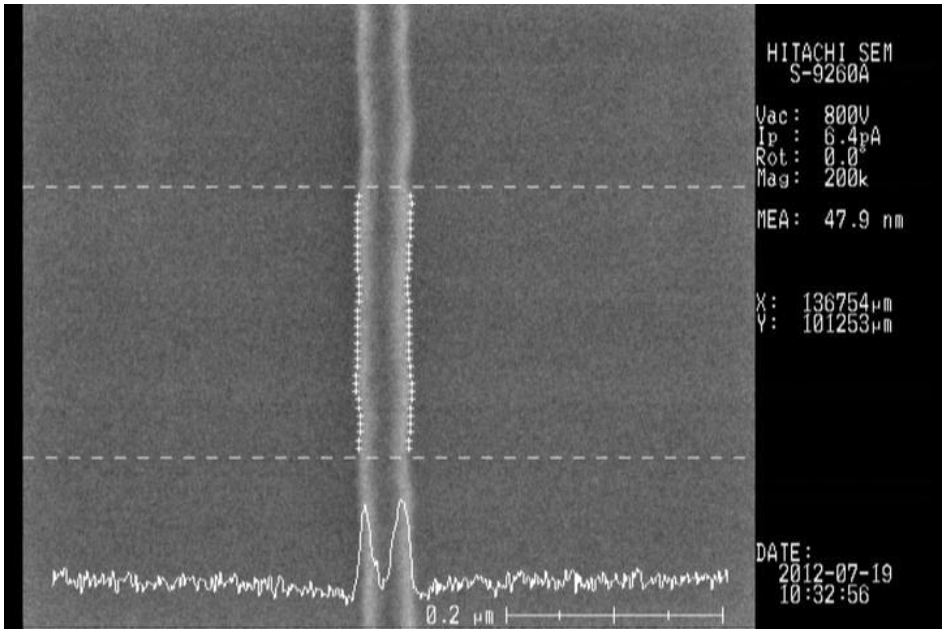
CAN resist process sequence aim: ~100nm resist thickness

NARLabs

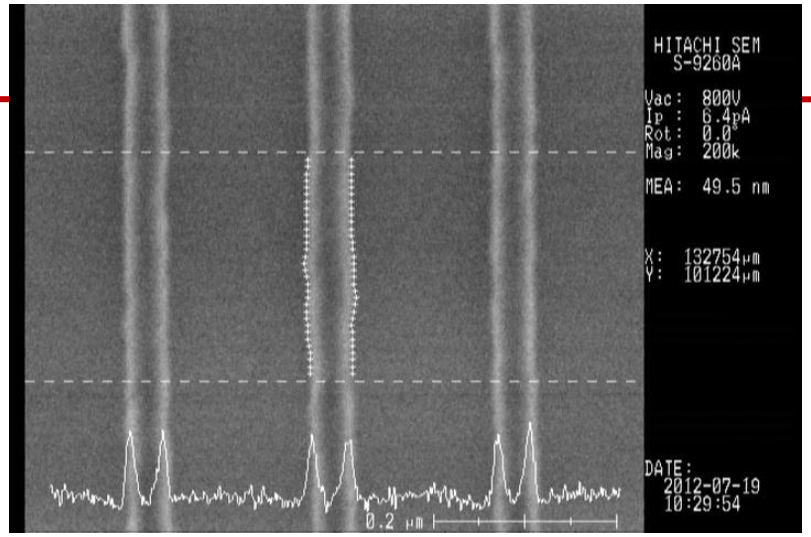
• Prime	HMDS 90°C
• Coating	1500 rpm 30“
• Softbake	110°C 90“
• Exposure	Base Dose 80μC/cm²
• Post Exposure Bake	110°C 60“
• Development	AD-10 2.38% TMAH 30“ puddle
• Rinse	Di-Water
• Hardbake	110°C 60“

  – Track ACT8 recipe
    - COT-CAN
    - DEV-CAN

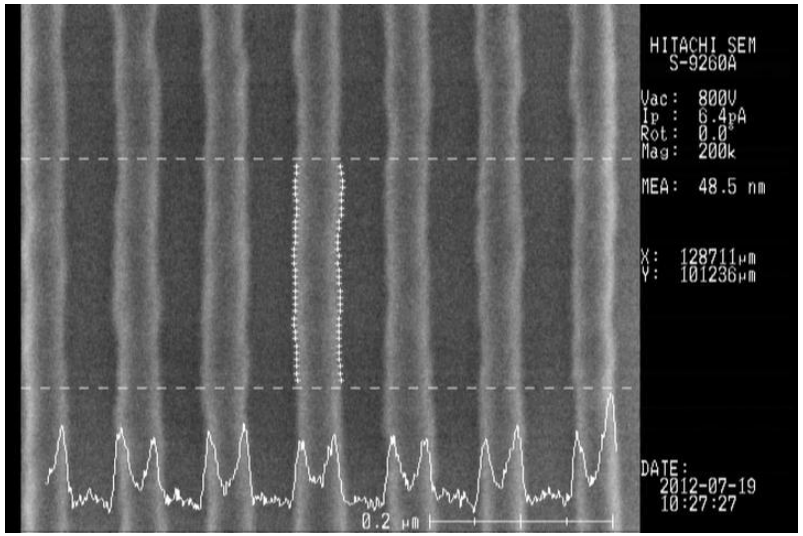
50 nm line



47.9 nm iso @80µC/cm²



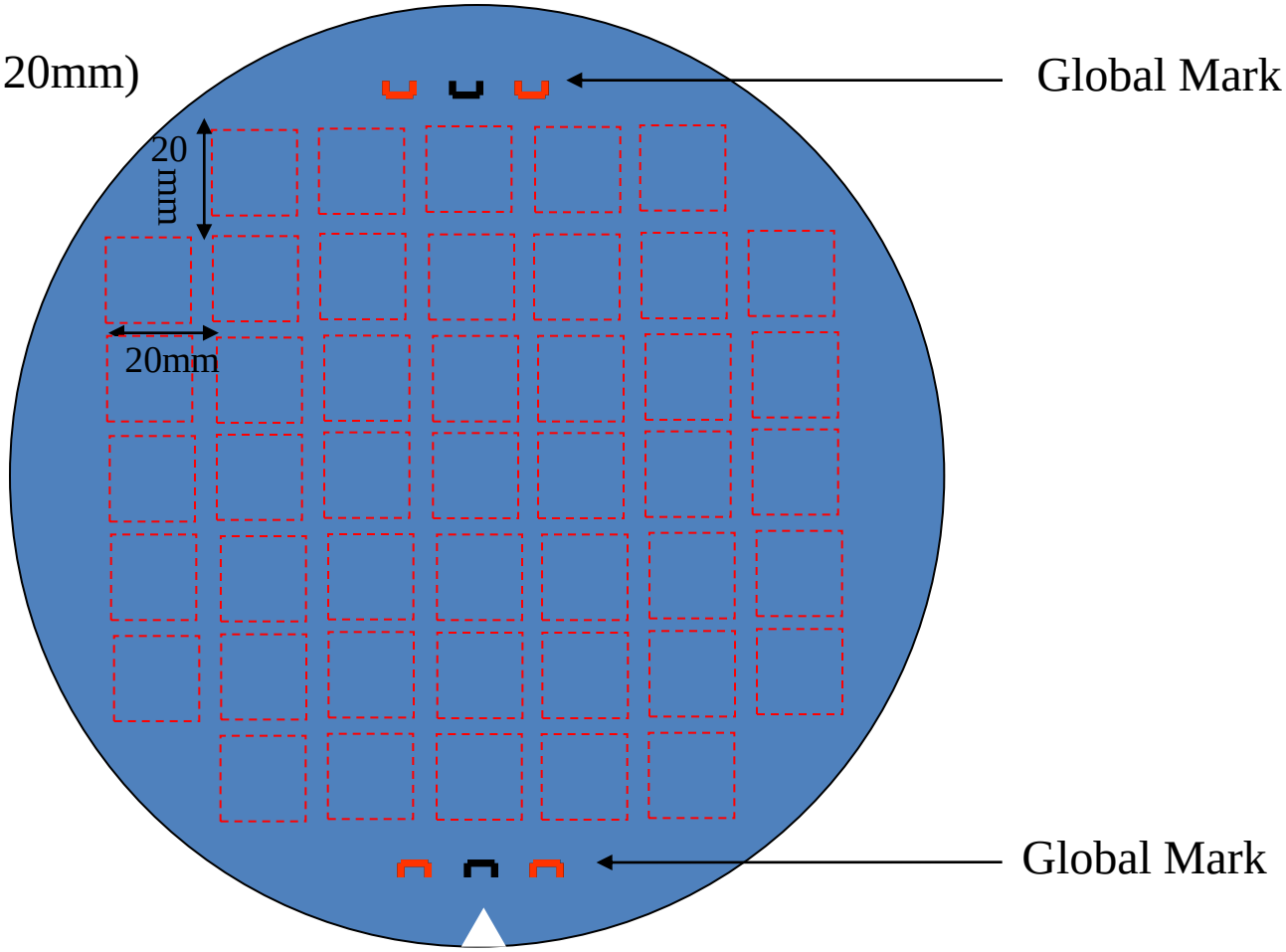
49.5 nm L/S=1:3 @76µC/cm²



48.5 nm L/S=1:1 @72µC/cm²

Chips placement on 8-inch wafer (standard layout)

Total 45 chips
Die pitch (20mm, 20mm)



Chip mark arrangement in the chip