Oerlikon DSE ICP Etcher 技術資料

● Process Baseline Check

Chamber Temp : 150~175℃
Elect Temp : -10~10℃
He clamp : 3500 mTorr
Process :TMD(Time Division Multiplex) Deep Si Etch process

● SPEC

All the process baseline have to measure with pattern wafers
Wafer structure: I-line mask or Oxide HM / Si substrate
*Poly-Si(undoped): E/R > 6um/min, Unif. < 15%
*Single-Si/PR selectivity > 50
*SEM poly-Si line: angle > 88°

● Bosch Process

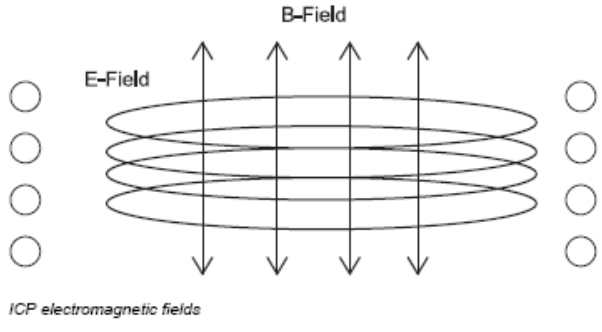


Figure 1

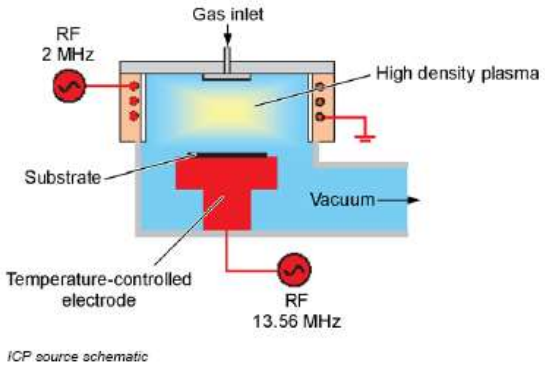
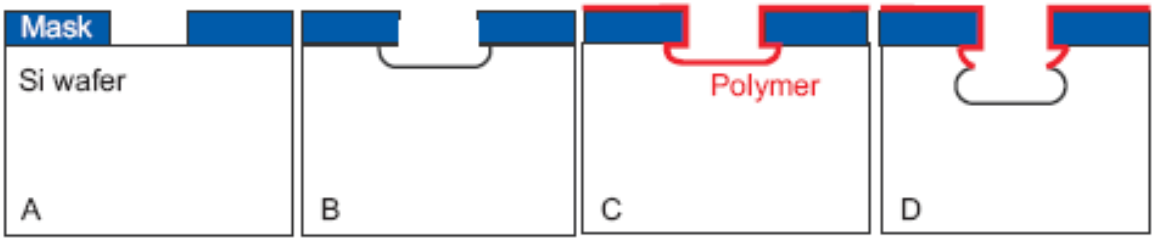


Figure 2

Oerlikon Versaline ICP Reactor is based on a cylindrical inductive coil configuration and inducing a strong magnetic field to generate a high density plasma source like Fig. 1 and Fig. 2.



Time Division Multiplex Etch Process

A Silicon wafer with patterned mask
B First etching cycle
C Passivation cycle
D Second etching cycle

The DSE Technology is based on the well-known time division multiplex (TDM) etch process. The TDM process employs alternating deposition (passivation) and etching as in Fig.3 (A~D). This process can be developed to achieve extremely high aspect ratio features on silicon substrates and TSV(Through-Si-Vis) technology.